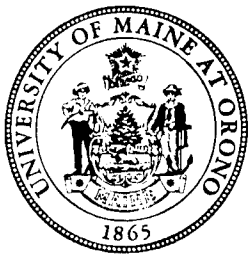
TECHNICAL REPORT FOR GRANT No.:
N00014-93-1-1007

University of Maine

ADC TEST SUPPORT PROGRAM
1 Nov 93 through 31 Oct 94

P.I. Fred H Irons
co-P.I. Donald M. Hummels



DEPARTMENT OF ELECTRICAL ENGINEERING

UNIVERSITY OF MAINE AT ORONO

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Principal Investigator: Fred H Irons
co-Investigator: Donald M. Hummels

Summary

This report summarizes accomplishments made under Grant No.: N00014-93-1-1007 for providing ADC Test Support to the ARPA HBT/ADC technology development program during the period of 1 Nov through 31 Oct 94. The following were accomplishments for this period. 1) Recruited and trained one graduate assistant to study ADC architectures and error modeling procedures. 2) Participated in the ARPA HBT/ADC design review on 26 Apr 94 and presented initial results relating ADC error basis functions to specific error phenomena. These results represent new procedures and ways to characterize ADCs based upon architectural error models. 3) Recruited an advanced graduate student in Jun 94 to begin implementation of orthogonal search procedures to facilitate ADC error modeling with the use of many-element basis sets. This student has recently started to develop simulation procedures for Delta-Sigma ADC architectures and their error effects. 4) Visited Lincoln Laboratory on 28 Jul 94 to review status of probe testing hardware development and prototype testing and evaluation plans. 5) Obtained and evaluated raw data samples obtained from Lincoln Laboratory for a 4-bit TRW prototype sampled at 1 GHz. 6) Wrote and submitted two papers for the 1995 IEEE International Symposium on Circuits and Systems dealing with ADC error modeling procedures developed under this program.

1. Introduction

The objective of this program is to support the ARPA Heterojunction Bipolar Technology/Analog-to-Digital Converter (HBT/ADC) program with independent component testing and evaluation. The University of Maine will collaborate with the HBT/ADC contractors, ARPA, MIT Lincoln Laboratory, and the Mayo Foundation to establish packaging and measurement guidelines for the independent testing of components developed under the ARPA program. In addition, this program is to give some consideration and support to the application of high performance ADCs to new and developing commercial and military applications.

This report summarizes accomplishments for the period spanning 1 Nov 93 through 31 Oct 94. It should be pointed out that there was a funding gap over this same period and the gap spanned the period from 1 Nov 93 to 25 May 94. Nevertheless, in Sep 93, a top ranking graduate student was recruited, assigned to this program, and trained in the modeling and understanding of different ADC architectures. This student was instrumental in helping to obtain results presented at the April 94 ARPA review and he is now currently deeply involved with Folding Amplifier Interpolating structures that are proposed for the 3-GHz ADC designs.

A second student was recruited at the beginning of the 1994 Summer Session. This second student possesses advanced software programming skills and expertise particularly in dealing with extra large numbers of unknowns in the parameterization of iterative solutions to complex problems. This assistant is involved with constructing more elaborate search techniques to solve for ADC error functions and in addition, he is developing a framework for simulating and studying the error effects of the Delta-Sigma converter which is proposed to be used in a 100 MHz, 12-bit ADC design. This is an important step for our effort, as we have not previously considered the use of the Delta-Sigma architecture in our modeling of ADC errors.

We have maintained close contact with Lincoln Laboratory over the past year so as to understand the progress of program specific prototype developments, to participate in the evaluation of measured data, to keep abreast of design tradeoffs that are being made with regard to ADC architectures, and to share results from the development of new test procedures as they occur in our program.

The remaining discussion provides more details for program accomplishments as listed in the above Abstract for this report.

2. UMaine Contribution at the April Review

The UMaine contribution to the past April Review for the HBT/ADC program is reviewed in this section. Several new concepts for understanding the characterization of ADC errors were presented at this meeting.

A highlight for the year was the discovery that one error function could be used to compensate different ADCs of the same production model, or type. For many years, the value of dynamic compensation has been regarded with suspicion due to the opinion that complex error functions would have to be determined for each ADC, and also that error functions would have to be periodically updated in order to be of any value. Since the published procedures have generally involved lengthy post-processing of large amounts of data, ADC designers have not pursued these procedures with much hope that they would be very useful. However, the determination of error as a function of signal state and slope has progressed to the point where generic system errors are accurately represented by current error functions and test procedures. At least this was found to be true for the 8-bit Tektronix AD20 tested at a sampling frequency of 204.8 MSPS.

The graph shown in Fig.1 presents measured results for the TKAD20 using test signals that span the first Nyquist band. The graph shows the spurious free dynamic range (SFDR) for both compensated and uncompensated data. The SFDR is one figure of merit used to characterize the dynamic performance of an ADC.

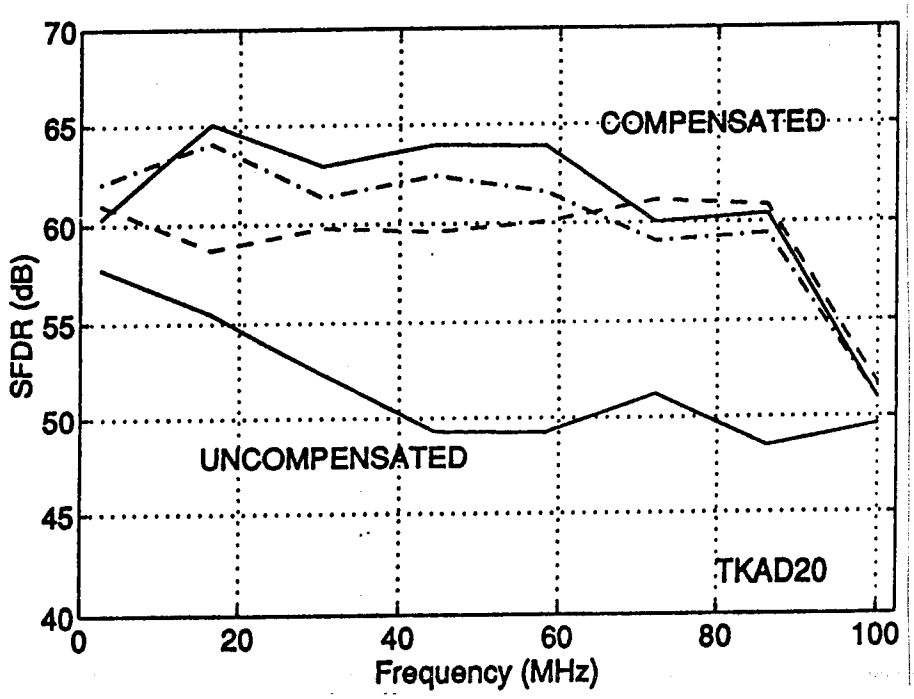

Fig.1 SFDR for three ADCs using the same error model

The ADCs used to obtain the data shown in Fig.1 came from two different production batches separated by more than a year in time. A single error function is used to compensate each of the ADCs with the result that improved performance is obtained for each ADC over a signifigant portion of the Nyquist band. These results show that integrated circuits replicate inherent dynamic error mechanisms and provide repeatable performance from batch to batch. An important corollary is that the cost of obtaining one error table can be spread across the application of many ADCs.

A paper which outlines the current calibration procedure is given in Appendix 1. The paper, entitled, *Characterization of ADCs Using a Non-iterative Procedure*, was submitted in Oct 93 and presented to the IEEE International Symposium on Circuits and Systems at London in May, 1994. The paper documents the equations and procedures used in the calibration problem and presents initial results obtained for the compensation of more than one ADC from a single error function. A second paper, which supplies more details about the calibration data and the use of a single two-tone calibration signal vs. several single-tone signals, is presented in Appendix 2. The paper, entitled, *Two-tone Characterization of Analog-to-Digital Converters*, was submitted in Mar 94 to the IEEE Midwest Symposium on Circuits & Systems and subsequently withdrawn when it was determined that no authors could attend to present the paper in August 94 at Lafayette, Louisiana. In Oct 94, The paper was re-submitted for presentation at the 1995 IEEE Symposium on Circuits & Systems to be held in Seattle next May. This paper helps to illustrate the use of the procedures outlined in paper No.1 and it shows that a single two-tone calibration signal yields an error function that works nearly as well as a table obtained from an extensive set of single-tone test signals. The payoff is that the calibration process can be performed with significantly less raw data and computation time and space, thus further enhancing the value of the compensation process.

Additional results, presented at the April review, included examples showing how our ADC calibration process can be used to obtain specific error effects due to how an ADC works. The procedure involves the selection of specific basis functions to represent error based upon mathematical models for different phenomena. One example showed how a table could be obtained to measure hysteresis effects only. Pulse basis functions were used with one set for positive slope signals and another set for negative slope signals. Sine wave calibation signals were found to be adequate to measure a hysteresis effect for a real ADC (The TKAD20). These results represented unique procedures that have recently emerged as a consequence of our beginning to formalize the understanding of the ADC in terms of architectures and error mechanisms. A second example considered amplitude dependent errors that arise from sample-time errors due to a simple Track-and-Hold model for the front end of an ADC. The model yielded a basis consisting of a linear function of state times the slope. When effects of nonlinear capacitance, encountered on the flash comparators, was considered, it was found that the error basis includes the model for the Track-and-Hold within a polynomial in the state

variable times the slope of the sampled signal. Thus two effects were found to be inseparable but their combination could be measured vs state by simply selecting appropriate basis functions and building an error table. Measured data on the subject TKAD20 showed that the hypotheses yielded consistent data. The resulting data showing Estimated Sample-Time error vs State were obtained from the calibration process without having to build any special timing circuitry or develop any new test procedures. The measured data also showed that the effects of sample-time error affect the upper end of the Nyquist band (for a good ADC) whereas the hysteresis affects the static, or low end of the Nyquist band as was expected.

The procedures developed to isolate specific dynamic errors through the use of basis function models are documented in a third paper included here in Appendix 3. This paper, entitled, *ADC Dynamic Error Modeling*, was submitted in Oct 94 to the 1995 IEEE International Symposium on Circuits & Systems. The paper documents the above results in more detail than was possible to present at the April meeting. The paper also provides further examples of using the procedures outlined in the first paper.

The above comments cover the contents of what was presented at the April review meeting. The three papers enclosed in the Appendix provide additional documentation for the procedures that are being organized to be able to analyze ADC components for specific errors based upon architectural considerations. So far the results are very encouraging and we are excited about the detail that can be extracted about internal parts by using only external measurements.

3. Review of TRW 4-bit ADC Prototype Performance

Sample data were obtained from Lincoln Laboratory so that we could apply some of our tests to the data. The prototype is a trial run for the process, but it is our understanding that other designs are planned for subsequent prototypes as scheduled in the program.

Enclosed are four graphs to indicate some performance measures for the prototype. The device was sampled at 1 GSPS and the graphs are based upon 16K samples per test frequency. The first two graphs are time Modulo plots based upon a test frequency of 399.23 MHz. Fig.2 shows the error obtained after excising the 20 largest harmonic components from the FFT spectrum of the sample set and then taking the inverse transform of the result. The error is free of harmonic distortion and should represent only random components due to quantization and sample time jitter. The error is compared to the sample values divided by 16, the binary to decimal range for a 4-bit converter, and a curve obtained from the second through sixth harmonic distortion terms as determined from the FFT of the sample set. The error is concentrated between ±1 LSB as it should be for an ideal quantizer with uniform dither set to cover a 1 LSB range. There are a few outlying error points due to statistical probability for a process which is not strictly uniform. The stair

step curve represents scaled sample values and it shows when the states are increasing and decreasing. The harmonic error constructed from the first five harmonics shows that the harmonic error is much less than 1 LSB and that the distortion is different for increasing vs decreasing state values; i.e., the device has some hysteresis.

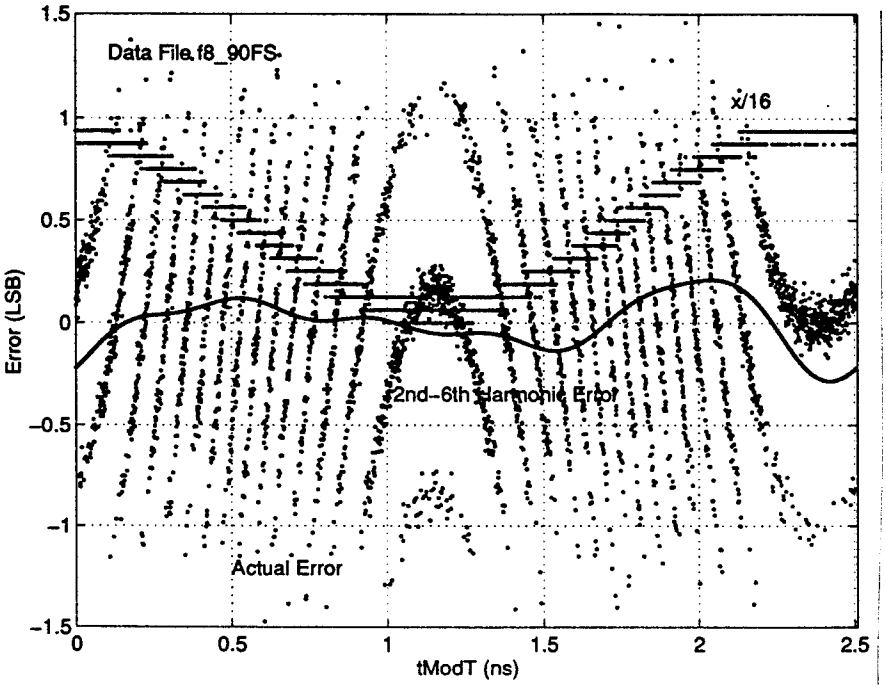

Fig.2 Error and sample values Modulo signal period

Fig.3 presents the same data in a slightly different form. The distortion free error is plotted versus the state of the ADC as estimated by using the fundamental component of the test data. This plot shows the classic error plot for a quantizer except that the range of the error is increased by the random dither used in the test. It also shows that that there is a concentration of samples in the the high and low states which is characteristic of a sinusoidal signal. When the distortion obtained from the 2nd through 6th harmonics is plotted against the fundamental component a Lissajous pattern is obtained which shows the hysteresis that is present in the device at this test frequency. If there were no hysteresis present, the curve would present a closed contour rather than an open contour for this test.

Sufficient data were taken to build an error function for this 4-bit converter and a compensated vs uncompensated SFDR was obtained. The result is shown in Fig.4 where it is seen that the device is capabable of being compensated and that it is performing close to an 8-bit dynamic range, i.e., 50 dB. It is expected that more range could be obtained by using smaller calibration signals, or by lowering the dither, so as to not drive the device into saturation and cutoff, i.e., avoid the states 0 and 15.

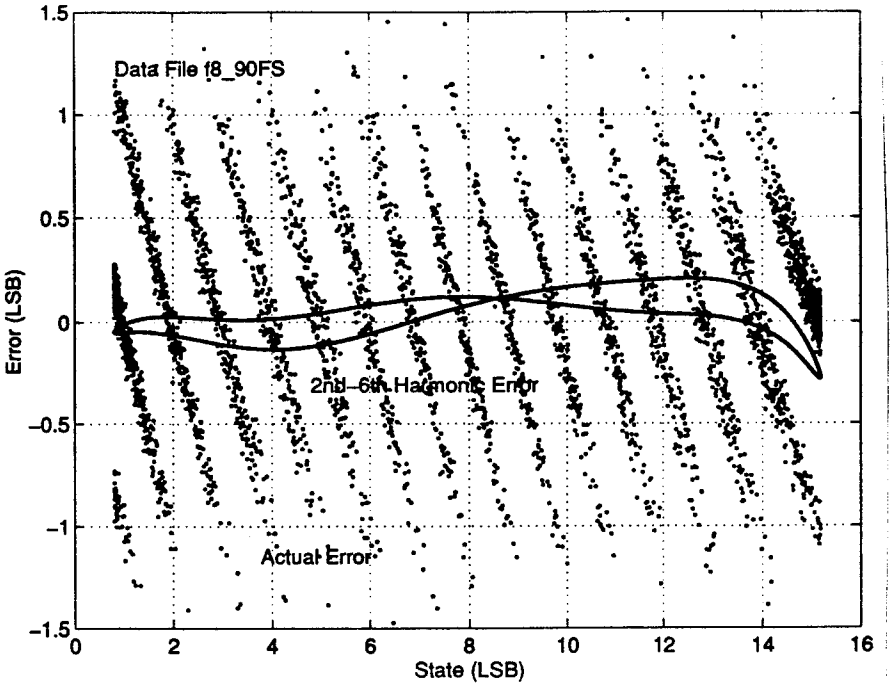

Fig.3 Error vs fundamental component of signal

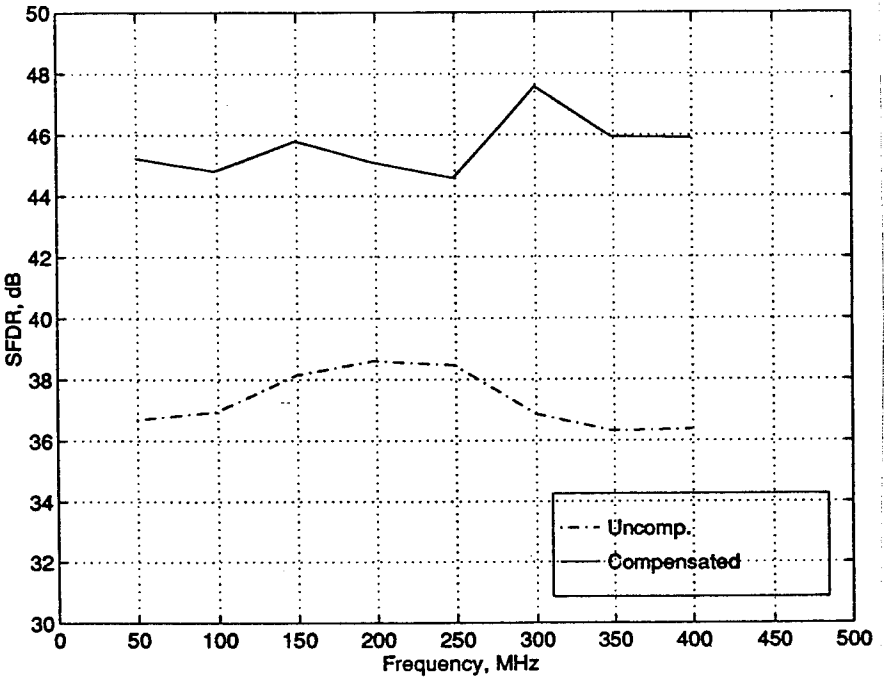

Fig.4 SFDR for TRW 4-bit prototype

The distortion free error consists primarily of random processes, however, if the device has amplitude dependent jitter such as may depend upon the slew rate of the test signal, then there will be random errors that correlate with each other at the second harmonic of the test signal. An experiment was developed to test this phenomena and an example result is shown in Fig.5 for this prototype device. The data shown in Fig.5 are derived from 4K sample sets at a test frequency of 405.517 MHz and a sample frequency of 1 GSPS. The data show that the sample time jitter

component is about 25 dB below the random dither and quantization error components (DC component). This result is consistent with trying to use the design to obtain another 4-bits of range. The graph shown in Fig.5 was obtained from the FFT of the square of the distortion free sample set plotted as actual error in Fig.2.

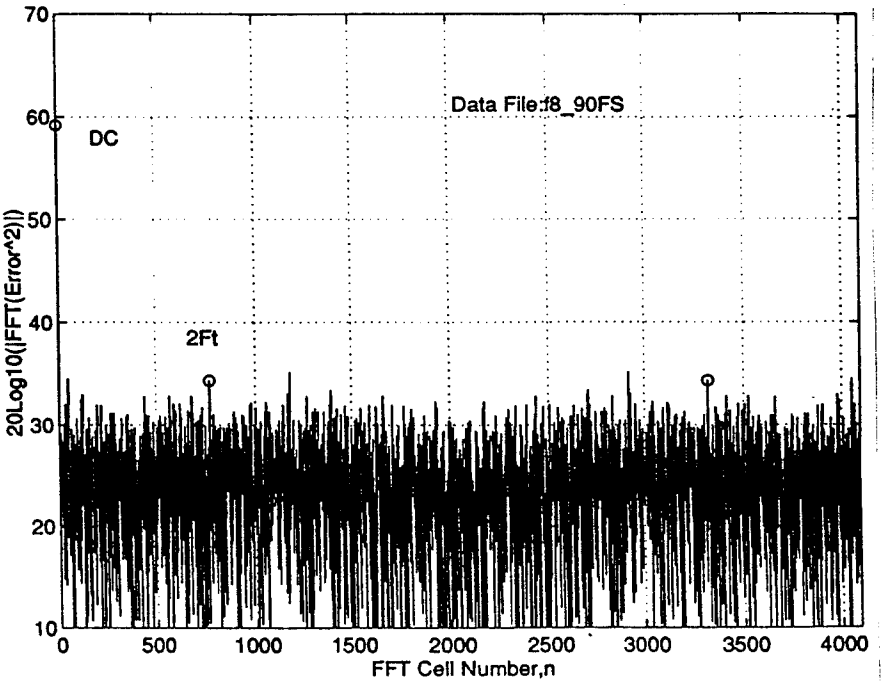

Fig.5 FFT magnitude spectrum for the error squared

The tests for obtaining statistical measures for the ADC random error components are just being developed as we organize tests to understand ADC architechural error mechanisms. A paper that gives more details about the process has been written and submitted to the 1995 IEEE International Symposium on Circuits & Systems and a copy of it is included in Appendix 4. The paper is entitled, *Measurement of Random Sample Time Jitter for ADCs*.

From a preliminary view, the data are consistent for the 4-bit design to be extended to attempt to obtain an 8-bit device. It would be useful however to see how the performance holds up as the sample frequency is increased. That is hopefully exactly what we will be able to do as our data acquisition capability gets upgraded to a higher level.

4. Applications

Part of our program objective is to consider applications of high performance ADCs. To this end nothing definite has been established but we are in dialogue with companies like Tektronix, Sanders/Lockheed, and MITRE. In connection with MITRE, steps were taken last July to establish a cooperative effort that will enable a graduate student to look at the issues between normal uniform dither and clutter-like background noises that are encountered in radar applications. To date our work has not considered this difference but there is some work that has been done at MITRE that illustrates a difference between the two approaches. We would like to understand this difference and determine whether or not specific types of dither signals offer advantages for the determination of errors. Conceptually it does not seem that error should depend upon application but it can depend upon the device as we already suspect in regard to the Delta-Sigma architecture where multi-tone signals are used to get intermodulation components to fall within the passband of the converter. It is expected that this cooperative program will be initiated sometime in early 1995.

5. Conclusion

This report has summarized accomplishments achieved over the period of 1 Nov 93 through 31 Oct 94. Two students have been indoctrinated to the program and its goals. They have made good progress toward the understanding and measurement of ADC architectural errors through the selection of error specific basis functions. These techniques have been applied to the development of new tests and evaluation procedures. Results are being documented with published papers to accomplish a technology transfer to the ADC design community.

There are two issues at which we are directing our current effort. One is to look at and understand specifics about the architectures that have been proposed by different vendors and the second is to try and determine what phenomena is dominant for improving the midrange of the Nyquist band performance for the flash type converters. So far, isolated phenomena improve either the low (static) or high ends of the Nyquist band. The flash converter is a building block for other types and we need to continue the understanding of architectural error sources, particularly for the folding and interpolating types of circuits. The Delta-Sigma, or algorithmic approach has not received much of our attention in past compensation work so we are directing effort on this architecture to try and determine what dynamic compensation procedures will best isolate its error sources. This architecture presents a challenge since many of the harmonics of single tone sources are filtered out by the decimation filters (harmonic aliasing is affected) however, it is expected that intermodulation testing using multiple-tone sources shold isolate implicit harmonic distortion mechanisms.

Appendix 1

A copy of Paper No.1, *Characterization of ADCs Using a Non-Iterative Procedure*, by DM Hummels, et al, was presented at the IEEE International Symposium at London, England in May 1994.

The paper documents the equations and procedures used in the ADC calibration problem.

Characterization of ADCs Using a Non-Iterative Procedure

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ABSTRACT

This paper describes procedures to obtain optimum error models for ADCs using a non-iterative technique. The goal of "phase-plane" compensation for ADCs is to determine the error which is introduced by a converter as a function of the ADC state and the (estimated) slope of the input signal. Past calibration schemes have been frustrated by uncertainties about the input calibration signal. In this paper, the error characteristic is expressed as a linear combination of a set of basis functions, which is then optimized to minimize the harmonic distortion in the output sample sequence. Degradation in performance due to inaccurate estimates of the input signal is avoided. The theories developed in this paper are applied to an 8-bit ADC sampling at 204.8 MSPS. Experimental results show that dynamic range performance can be improved by as much as 12 dB over the Nyquist band. A further interesting result is that an error function measured for one ADC is found to work equally well for another ADC taken from the same production run. The errors determined are thus found to be unique to the ADC design and production, and not to the test and representation methods. It is believed that this is the first time that results of this nature have been reported in the literature.

1 INTRODUCTION

Dynamic error correction methods for analog-to-digital converters (ADC's) have been under development for several years. The motivation for dynamic error correction is to eliminate frequency dependent distortion introduced by analog to digital converters. ADC manufacturers typically limit distortion power levels introduced by an ADC to values on the order of the quantization error power. This distortion typically limits the spurious free dynamic range (SFDR) of an ADC to approximately $6n$ dB, where n is the number of bits in the converter. That is, the distortion introduced by quantizing a near full scale sine wave will cause spurious harmonics at power levels which are approximately $6n$ dB below the input power level. Many applications, however, require dynamic range far in excess of this value. One such application is the use of wide bandwidth ADC's on the input of digitally implemented communication or radar receivers. Here, nonlinearities in the signal path are often dominated by the ADC, limiting the achievable dynamic range of the receiver.

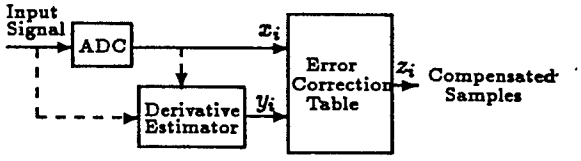

Figure 1: ADC Compensation Architecture

Researchers have known for some time that the distortion introduced by an ADC is a dynamic phenomenon, and that simply applying a fixed correction to each ADC output improves the SFDR of the converter only near the calibration frequency [1]. Dynamic compensation procedures have been introduced to cope with this frequency dependent distortion. These techniques typically base the error correction on the current output of the converter and some estimate of the slope of the input signal at the time that the sample was taken. Figure 1 illustrates the approach, in which values of an error function are stored in a memory which is accessed by the state and slope of the input signal. A number of techniques have been used to derive the slope estimate. Slope estimates may be obtained either by processing the ADC output sample sequence or by adding additional analog circuitry/converters to obtain the information directly from the input signal.

An ADC calibration procedure is required to determine the error correction table entries. Initial compensation schemes approximated the error introduced by the converter by estimating the amplitude and phase of the input calibration signal using a mean-square fit to the *output* sample sequence. Simulation studies [3, 4] have shown that inaccuracies in these estimates cause a significant degradation in performance as the ADC input frequency deviates from the calibration frequency. Iterative procedures have been introduced which vary the assumed amplitude and phase until an acceptable table is formed [3, 4]. These techniques improve the performance of the compensated converter, but are computationally expensive, and may never converge to a solution.

This paper describes a direct, non-iterative, procedure to determine the error function for an ADC. Section 2 introduces the notation and gives the theoretical formulation of the calibration procedure. The procedure is not specific to the form of the derivative estimator, and may be extended to more general compensation architectures. Section 3 presents the measured performance of the algorithm for an 8-bit 204.8 MSPS converter.

2 COMPENSATION FORMULATION

The compensation problem will be formulated under the assumption that two variables are used to index the error correction table. As in past dynamic compensation efforts, the first index into the error table will be assumed to be the ADC state, and the second is generally a quantity which is related to the derivative of the input signal at the sampling instant. Although the extension to error tables with more inputs is straightforward, previous efforts in this direction have not improved performance beyond that obtained with the two-input tables [5].

Let x_i represent the ith sample taken by the ADC, and y_i the quantity which is to be used to index the second axis of the table. We denote the compensated signal by z_i, where z_i is given by

$$z_i = x_i - \mathrm{e}(x_i, y_i) \tag{1}$$

The goal of compensation is to linearize the converter, so that the sample sequence z_i is an accurate rendition of the ADC input. An ADC calibration procedure is required to determine the unknown function $\mathrm{e}(x, y)$.

To calibrate the converter, the ADC is excited using a pure sinusoidal calibration signal with known frequency f_0. Because of unknown gains and delays before the input stages of the converter, the exact amplitude and phase of the input calibration signal is not generally known. Past calibration procedures have emphasized estimation of the ADC input from the output sample sequence. As pointed out in [2], estimation procedures based on finding the minimum mean-square error fit to the output sequence are generally inadequate, resulting in a degradation of performance as the ADC input frequency moves away from the calibration frequency. Iterative procedures were introduced for which the assumed amplitude and phase of the calibration signal is varied until an acceptable table is obtained. Here, we formulate the calibration problem such that estimation of the input signal is not required, resulting in a more accurate error correction table in a fraction of the time required for the iterative procedure.

Let $\vec{x} = [x_1\ x_2\ \ldots\ x_N]^T$ represent a vector of ADC output samples collected by sampling the sinusoidal calibration signal with sampling frequency f_s. Further, let $\vec{y} = [y_1\ y_2\ \ldots\ y_N]^T$ be the corresponding vector of values used to index the second axis of the table. The vector of compensated values is

$$\vec{z} = \vec{x} - \vec{\mathrm{e}}(\vec{x}, \vec{y}) \tag{2}$$

where

$$\vec{\mathrm{e}}(\vec{x}, \vec{y}) = \begin{bmatrix} \mathrm{e}(x_1, y_1) \\ \mathrm{e}(x_2, y_2) \\ \vdots \\ \mathrm{e}(x_N, y_N) \end{bmatrix} \tag{3}$$

The goal is to select $\mathrm{e}(x, y)$ to minimize the distortion in $\vec{z}$. For the calibration signal, the distortion in $\vec{z}$ may be measured by evaluating the DFT of the sequence $\{z_1,\ z_2,\ \ldots,\ z_N\}$ at the harmonics of the input calibration frequency. Let $\widetilde{T}$ denote the transformation matrix which gives the second through the Mth harmonic of the input signal:

$$\widetilde{T} = \begin{bmatrix} W^0 & W^2 & W^4 & \ldots & W^{2N} \\ W^0 & W^3 & W^6 & \ldots & W^{3N} \\ W^0 & W^4 & W^8 & \ldots & W^{4N} \\ & \vdots & & & \\ W^0 & W^M & W^{2M} & \ldots & W^{MN} \end{bmatrix} \tag{4}$$

where

$$W = e^{j2\pi f_0/f_s} \tag{5}$$

Then $\widetilde{T}\vec{z}$ is the vector which contains the 2nd through the Mth harmonics measured in this manner. We wish to determine the function $e(x, y)$ which minimizes $||\widetilde{T}\vec{z}|| = ||\widetilde{T}\vec{x} - \widetilde{T}\vec{\mathrm{e}}(\vec{x}, \vec{y})||$ by solving the system of equations

$$\widetilde{T}\vec{x} = \widetilde{T}\vec{\mathrm{e}}(\vec{x}, \vec{y}) \tag{6}$$

in the least-squares sense.

To solve for the function $e(x, y)$, we first write the function as a linear combination of L (known) basis functions $b_i(x, y)$:

$$e(x, y) = \sum_{i=1}^{L} \alpha_i b_i(x, y) \tag{7}$$

The optimization problem is to select the best values for $\alpha_1, \alpha_2, \ldots, \alpha_L$. Let $\vec{b}_i(\vec{x}, \vec{y})$ denote the vector of values obtained from the ith basis function evaluated at each of the calibration (x_i, y_i) pairs:

$$\vec{b}_i(\vec{x}, \vec{y}) = \begin{bmatrix} b_i(x_1, y_1) \\ b_i(x_2, y_2) \\ \vdots \\ b_i(x_N, y_N) \end{bmatrix} \tag{8}$$

Then the vector of error table values is given by

$$\vec{e}(\vec{x}, \vec{y}) = \sum_{i=1}^{L} \alpha_i \vec{b}_i(\vec{x}, \vec{y}) \tag{9}$$

$$= \tilde{B}\vec{\alpha} \tag{10}$$

where $\tilde{B}$ is a $N \times L$ matrix with (i, j) element given by $b_j(x_i, y_i)$, and $\vec{\alpha} = [\alpha_1\ \alpha_2\ \ldots\ \alpha_L]^T$. Using a basis function representation for $e(x, y)$ presents a classical linear least-squares problem. Substituting (10) into (6) gives

$$\tilde{T}\tilde{B}\vec{\alpha} = \tilde{T}\vec{x} \tag{11}$$

The least-squares solution to (11) is obtained by multiplying both sides of the equation by the pseudo-inverse of $\tilde{T}\tilde{B}$. In implementation, the entries of the $(M-1) \times L$ matrix $\tilde{T}\tilde{B}$ are calculated directly using FFTs of each of the vectors $\vec{b}_i(\vec{x}, \vec{y})$, rather than calculating the (large) matrices $\tilde{T}$ and $\tilde{B}$ separately. The singular-value decomposition is then used to evaluate the pseudo-inverse of the matrix. Values of $\tilde{T}\vec{x}$ are obtained directly from the FFT of $\vec{x}$.

Note that although the above discussion is cast in terms of a single calibration signal, in practice more than one calibration signal is used so that all possible (x, y) pairs are excited. In this case, each calibration signal gives a system of equations in the form of (11), and the solution is given by

$$\vec{\alpha} = \begin{bmatrix} \tilde{T}^{(1)}\tilde{B}^{(1)} \\ \tilde{T}^{(2)}\tilde{B}^{(2)} \\ \vdots \\ \tilde{T}^{(K)}\tilde{B}^{(K)} \end{bmatrix}^{+} \begin{bmatrix} \tilde{T}^{(1)}\vec{x}^{(1)} \\ \tilde{T}^{(2)}\vec{x}^{(2)} \\ \vdots \\ \tilde{T}^{(K)}\vec{x}^{(K)} \end{bmatrix} \tag{12}$$

where K is the number of calibration signals, and $\tilde{T}^{(i)}$, $\tilde{B}^{(i)}$, and $\vec{x}^{(i)}$ are the required matrices and vectors for each of the calibration signals, and $[\ ]^+$ denotes the pseudo-inverse of the indicated matrix.

3 EXPERIMENTAL RESULTS

The above algorithm was implemented using Gaussian basis functions with centers distributed on a 10×10 grid covering the range of possible (x,y) combinations. Each of the basis functions has the form

$$b_i(x, y) = e^{-\frac{1}{2}\left(\left(\frac{x-c_{xi}}{\sigma_x}\right)^2 + \left(\frac{y-c_{yi}}{\sigma_y}\right)^2\right)} \tag{13}$$

where c_{xi} and c_{yi} are the basis function centers and depend on i. The parameters σ_x and σ_y determine the "smoothness" of the basis functions. The parameters σ_x and σ_y were selected to be equal to the separation of the basis functions centers in the x and y directions respectively.

A Tektronix AD-20 eight-bit converter sampling at 204.8 MSPS was used to test the compensation algorithm. The converter was calibrated using 16 calibration signals (eight frequencies from 2.5 to 80 MHz at two amplitudes). It is important that the loci of $x-y$ pairs excited by the various calibration signals cross each other to avoid ambiguities in the error function solution. The output of a 31-tap FIR differentiating filter was used to provide the y-axis values for the error characteristic. For each of the calibration signals, N=4096 samples were collected and used to estimate the various harmonics required in (12). Equation (12) was formulated to minimize the first 20 harmonics of each of the signals. Compensation was accomplished by accessing values of the error function from an error correction table. The table was formed by evaluating $e(x, y)$ on a 128×128 grid on the $x - y$ plane.

Figure 2 illustrates the improvement in performance which is achieved by compensation. The figure shows the uncompensated and compensated spurious-free dynamic range (SFDR) for the converter tested at an input level of -1 dB relative to full-scale (-1 dBFS). The SFDR is measured by driving the converter with a pure sinusoidal signal, and measuring the dB difference between the height of the fundamental and the height of the highest spurious signal in the spectrum of the ADC output samples. In the figure, the SFDR is plotted for various input test frequencies across the Nyquist band. The figure shows that compensation is providing 10 dB or more improvement over the majority of the Nyquist band. The resulting 8-bit converter is providing over 60 dB

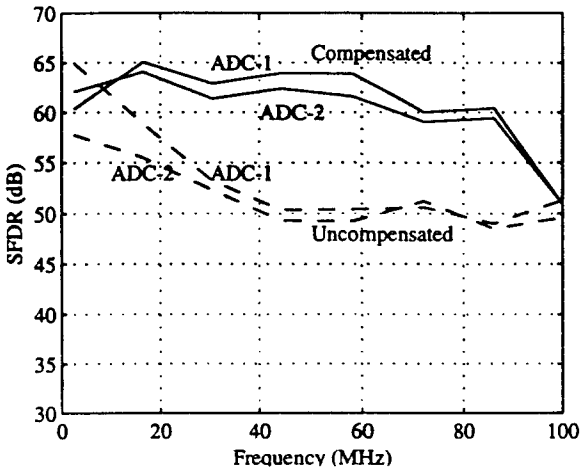

Figure 2: Spurious-free dynamic range (uncompensated and compensated) for two converters. Both compensated characteristics were obtained using the *same* error table, which was created by calibrating ADC-1.

of dynamic range from DC to 90 MHz. Above 90 MHz, the compensation performance drops back to that of the uncompensated converter, as the FIR filter fails to give a valid estimate of the slope of the input signal at these frequencies.

Note that the performance is uniformly good across the Nyquist band, not exhibiting the degradation which has been typical of other compensation algorithms. To a large extent, this result is a verification of the simulation results presented in [4], which suggested that a possible reason for the performance degradation was the inaccurate knowledge of the amplitude and phase of the input calibration signal. By not estimating the input signal from the output sample sequence, this problem is avoided in our formulation.

To test the generalization of the error characteristic to other converters manufactured in the same lot, a second Tektronix AD-20 ADC was compensated *using the table which was created by calibrating the first converter.* Figure 2 shows the resulting performance, labeled as 'ADC-2'. The compensated ADC gives performance which is nearly identical to that obtained by the original ADC which was used to obtain the error table. This is an important result, suggesting that the distortion which is introduced by the converter is primarily a function of the ADC design and production, and is generic from device to device. It suggests that manufacturers may be able to obtain correction tables which apply to a large number of converters by actually calibrating a relatively small number of devices.

4 CONCLUSIONS

This paper has introduced an approach to calibrating analog to digital converters which avoids the estimation of the amplitude and phase of the input calibration signal. Because iterative schemes to estimate the input are not used, the computational burden required by the algorithm has been greatly reduced. (For our workstation, the required time for constructing the table has dropped from over ten hours for the techniques reported in [2] to just over three minutes for the algorithm presented here.) The resulting tables actually out-perform tables created using previous techniques. Specifically, they do not exhibit the degradation in performance as test frequencies are moved away from the calibration frequency that are typical of techniques which require estimation of the input signal. Finally, the results show that a single error correction is not specific to the ADC used for calibration. Two ADCs from the same production lot were shown to be compensatable using the same error table, suggesting that manufacturers may be able to obtain correction tables which apply to a large number of converters by actually calibrating a relatively small number of devices.

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Appendix 2

A copy of Paper No.2, *Two-Tone Characterization of Analog-to-Digital Converters*, by IN Papantonopoulos, et al, was submitted in Oct 1994 for presentation at the 1995 IEEE International Symposium on Circuits & Systems.

The paper supplies more details about ADC calibration data and the use of a single two-tone calibration signal vs. several single-tone signals.

Two-tone Characterization of Analog-to-Digital Converters

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***Abstract*— This paper introduces an ADC calibration procedure requiring only a single two-tone calibration signal. The resulting intermodulation terms densely excite the phase-plane space of the converter, thus allowing for the construction of an accurate error table. Results from a real ADC are presented for the first time.**

I. INTRODUCTION

Dynamic error correction methods for analog-to-digital converters (ADC's) have been under development for several years [1, 2, 3, 4]. The motivation for dynamic error correction is to eliminate frequency dependent distortion introduced by analog to digital converters. ADC manufacturers typically limit distortion power levels introduced by an ADC to values on the order of the quantization error power. This distortion typically limits the spurious free dynamic range (SFDR) of an ADC to approximately $6n$ dB, where n is the number of bits in the converter. That is, the distortion introduced by quantizing a near full scale sine wave will cause spurious harmonics at power levels which are approximately $6n$ dB below the input power level. Many applications, however, require dynamic range far in excess of this value. One such application is the use of wide bandwidth ADC's on the input of digitally implemented communication or radar receivers. Here, nonlinearities in the signal path are often dominated by the ADC, limiting the achievable dynamic range of the receiver.

Researchers have known for some time that the distortion introduced by an ADC is a dynamic phenomenon, and that simply applying a fixed correction to each ADC output improves the SFDR of the converter only near the calibration frequency [5]. Dynamic compensation procedures have been introduced to cope with this frequency dependent distortion. These techniques typically base the error correction on the current output of the converter and some estimate of the slope of the input signal at the time that the sample was taken. Figure 1 illustrates the approach, in which values of an error function are stored in a memory which is accessed by the state and slope of the input signal. A number of techniques have been used to derive the slope estimate. Slope estimates may be obtained either by processing the ADC output sample sequence or by adding additional analog circuitry/converters to obtain the information directly from the input signal.

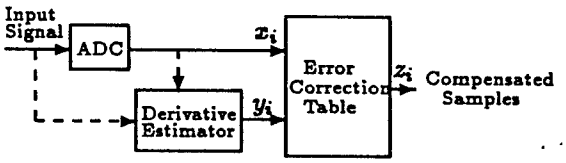

Figure 1: ADC Compensation Architecture

An ADC calibration procedure is required to determine the error correction table entries. In the past, calibration procedures have involved driving the converter using pure sinusoidal signals at various amplitudes and phases. Sinusoidal signals have been selected since they can be generated at high frequencies and filtered to obtain desired fidelity. In order to calibrate a converter, a variety of calibration signal amplitudes and frequencies are required in order to excite the device densely in the state-slope plane (the *phase-plane*). Implementation of the procedure would necessitate a complex function generator capable of generating the required frequencies and amplitudes, as well as a switchable set of filters. In this paper, we show that a single calibration signal may be used to cover the phase-plane. The signal is composed of two sinusoids with frequencies near the Nyquist frequency. Using this calibration signal requires only two (fixed frequency) oscillators, and a single filter.

In section II we show that the two-tone calibration procedure effectively excites the phase-plane. Section III presents the algorithm implemented for converter calibration with a two-tone signal. Experimental results for the procedures are presented in Section IV.

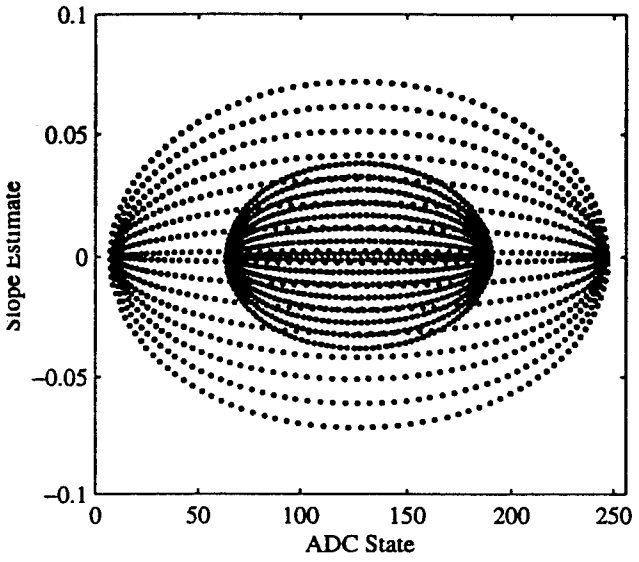

Figure 2: Phase plane trajectories for 16 single-tone calibration signals (2 amplitudes, 8 frequencies).

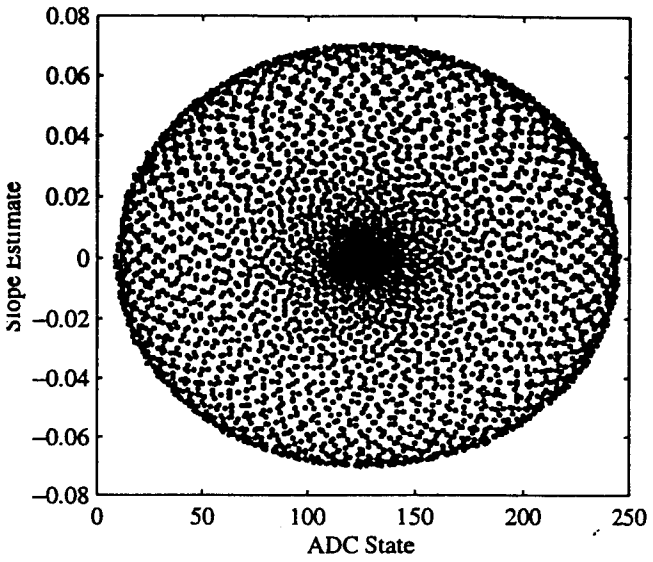

Figure 3: Phase plane trajectory for two-tone calibration signal.

II. The Calibration Signal

Figure 2 shows a scatter plot of the state and derivative trajectories of the single-tone calibration data, where 8 frequencies and 2 amplitudes per frequency were used. The data was collected from a Tektronix AD20 converter sampling at 204.8 MSPS. In comparison, Figure 3 shows the corresponding two-tone phase-plane excitation, where only one calibration signal was used. This plot shows that the converter's phase-plane can be very densely and uniformly excited by a two-tone signal. In order to excite as many state-slope pairs as possible, the two-tone signal frequencies should be chosen near the Nyquist frequency. The amplitudes of the two signals are set equal to each other, slightly below 50% of full scale.

III. Calibration Algorithm

The calibration algorithm follows closely the procedure presented in [6]. Let x_i represent the ith sample taken by the ADC, and y_i the slope estimate. We denote the compensated signal by z_i, where z_i is given by

$$z_i = x_i - \mathrm{e}(x_i, y_i) \tag{1}$$

The goal of compensation is to linearize the converter, so that the sample sequence z_i is an accurate rendition of the ADC input. An ADC calibration procedure is required to determine the unknown function $\mathrm{e}(x, y)$.

Assume that the converter is excited using a two-tone signal with frequencies f_1 and f_2. The converter distorts the signal, resulting in energy at a large number of intermodulation frequencies. Let $\nu_0\ \nu_1\ \ldots\ \nu_{M-1}$ be a subset of significant intermodulation frequencies of the form

$$\nu_i = k_1 f_1 + k_2 f_2 \tag{2}$$

Let $\vec{x} = [x_1\ x_2\ \ldots\ x_N]^T$ represent a vector of ADC output samples collected by sampling the sinusoidal calibration signal with sampling frequency f_s. Further, let $\vec{y} = [y_1\ y_2\ \ldots\ y_N]^T$ be the corresponding vector of values used to index the second axis of the table. The vector of compensated values is

$$\vec{z} = \vec{x} - \vec{\mathrm{e}}(\vec{x}, \vec{y}) \tag{3}$$

where

$$\vec{\mathrm{e}}(\vec{x}, \vec{y}) = \begin{bmatrix} \mathrm{e}(x_1, y_1) \\ \mathrm{e}(x_2, y_2) \\ \vdots \\ \mathrm{e}(x_N, y_N) \end{bmatrix} \tag{4}$$

The goal is to select $\mathrm{e}(x, y)$ to minimize the distortion in $\vec{z}$. For the calibration signal, the distortion in $\vec{z}$ may be measured by evaluating the DFT of the sequence $\{z_1,\ z_2,\ \ldots,\ z_N\}$ at the harmonics of the input calibration frequency. Let $\tilde{T}$ denote the transformation matrix which gives the components of the signal at each of the intermodulation frequencies:

$$\tilde{T} = \begin{bmatrix} W_0^0 & W_0^1 & W_0^2 & \ldots & W_0^{N-1} \\ W_1^0 & W_1^1 & W_1^2 & \ldots & W_1^{N-1} \\ W_2^0 & W_2^1 & W_2^2 & \ldots & W_2^{N-1} \\ & \vdots & & & \\ W_{M-1}^0 & W_{M-1}^1 & W_{M-1}^2 & \ldots & W_{M-1}^{N-1} \end{bmatrix} \tag{5}$$

where

$$W_i = e^{-j2\pi\nu_i/f_s} \tag{6}$$

Then $\tilde{T}\vec{z}$ is the vector which contains the 2nd through the Mth harmonics measured in this manner. We wish to determine the function $e(x,y)$ which minimizes $||\tilde{T}\vec{z}|| = ||\tilde{T}\vec{x} - \tilde{T}\vec{e}(\vec{x},\vec{y})||$ by solving the system of equations

$$\tilde{T}\vec{x} = \tilde{T}\vec{e}(\vec{x},\vec{y}) \tag{7}$$

in the least-squares sense.

To solve for the function $e(x,y)$, we first write the function as a linear combination of L (known) basis functions $b_i(x,y)$:

$$e(x,y) = \sum_{i=1}^{L} \alpha_i b_i(x,y) \tag{8}$$

The optimization problem is to select the best values for $\alpha_1, \alpha_2, \ldots, \alpha_L$. Let $\vec{b}_i(\vec{x},\vec{y})$ denote the vector of values obtained from the ith basis function evaluated at each of the calibration (x_i, y_i) pairs:

$$\vec{b}_i(\vec{x},\vec{y}) = \begin{bmatrix} b_i(x_1,y_1) \\ b_i(x_2,y_2) \\ \vdots \\ b_i(x_N,y_N) \end{bmatrix} \tag{9}$$

Then the vector of error table values is given by

$$\vec{e}(\vec{x},\vec{y}) = \sum_{i=1}^{L} \alpha_i \vec{b}_i(\vec{x},\vec{y}) \tag{10}$$

$$= \tilde{B}\vec{\alpha} \tag{11}$$

where $\tilde{B}$ is a $N \times L$ matrix with (i,j) element given by $b_j(x_i,y_i)$, and $\vec{\alpha} = [\alpha_1\ \alpha_2\ \ldots\ \alpha_L]^T$. Using a basis function representation for $e(x,y)$ presents a classical linear least-squares problem. Substituting (11) into (7) gives

$$\tilde{T}\tilde{B}\vec{\alpha} = \tilde{T}\vec{x} \tag{12}$$

The least-squares solution to (12) is obtained by multiplying both sides of the equation by the pseudo-inverse of $\tilde{T}\tilde{B}$. In implementation, the entries of the $(M-1)\times L$ matrix $\tilde{T}\tilde{B}$ are calculated directly using FFTs of each of the vectors $\vec{b}_i(\vec{x},\vec{y})$, rather than calculating the (large) matrices $\tilde{T}$ and $\tilde{B}$ separately. The singular-value decomposition is then used to evaluate the pseudo-inverse of the matrix. Values of $\tilde{T}\vec{x}$ are obtained directly from the FFT of $\vec{x}$.

IV. Results

A Tektronix AD20 converter sampling at 204.8 MSPS was compensated by means of an error table created from two-tone calibration. Figure 4 illustrates the comparative Spurious-Free Dynamic Range (SFDR) for the uncompensated, the single-tone calibrated and the two-tone calibrated converter. The two-tone procedure compensated the converter throughout the Nyquist band, yielding a maximum dynamic range improvement of 11 dB. Although the single-tone calibration is better in the lower end of the Nyquist band, the two-tone calibration compensates at least as well (if not better) around the high end of the band.

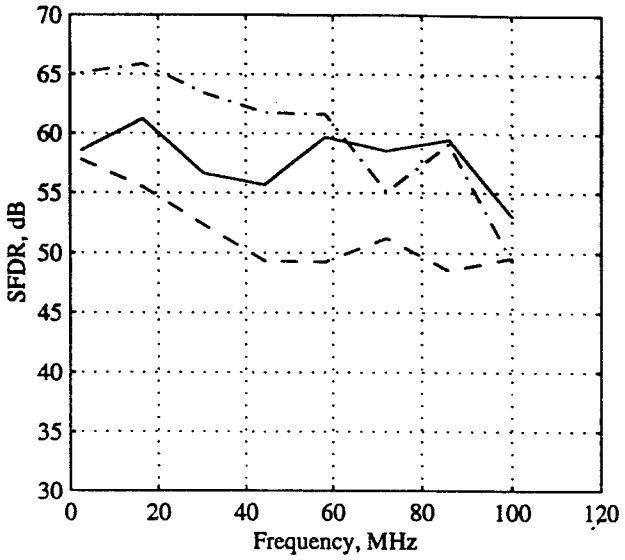

Figure 4: Spurious free dynamic range performance of uncompensated (dashed), single-tone (dash-dot), and two-tone (solid) calibrated converter.

V. Conclusions

This paper has introduced a new way to calibrate analog to digital converters which only requires a single two-tone calibration signal. The composite signal consists of two sinusoids, thus eliminating the need for multiple single-tone calibration signals and corresponding filters. The intermodulation terms uniformly excited the converter's phase-plane, yielding a much denser set of calibrating state-slope pairs. The converter's dynamic range was improved throughout the Nyquist band, yielding an SFDR performance comparable to that of single-tone calibration. The two-tone procedure yields a much more efficient calibration technique. It is also believed that this is the first time that such a technique has been reported and successfully tested on a real converter.

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Appendix 3

A copy of Paper No.3, *ADC Dynamic Error Modeling*, by FH Irons, et al, was submitted in Oct 1994 for presentation at the 1995 IEEE International Symposium on Circuits & Systems.

The paper illustrates methods developed to isolate specific dynamic errors through the use of basis function models and the calibration process.

ADC Dynamic Error Modeling

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Abstract— **Following published procedures for characterizing ADCs using phase-plane error functions, this paper shows how a given calibration data set may used to extract estimates of specific error performance features pertaining to ADC architectural considerations. The procedure requires the selection of basis functions based upon properties of a desired feature. The techniques are applied to the 8-bit TKAD20 operating at 204.8 MSPS to illustrate the concepts discussed in the paper. Results show how it is possible to estimate hysteresis and average sample time errors versus the state of the ADC. A simple consideration shows why it is not possible to separate sample time errors from the effects of nonlinear capacitance.**

I. Introduction

It has been reported [1] that the dynamic error representation for an ADC could be obtained in a direct fashion from a set of sine wave calibration data. The dynamic error is assumed to be a function of two variables, x and y, where x represents the output state and y represents an estimate of the corresponding slope of the state of the ADC output.

$$e(x,y) = \sum_{i=1}^{L} \alpha_i b_i(x,y) \qquad (1)$$

The error function given by (1) is represented over the space defined by x and y for the set of basis functions, b_i. Since y is a measure of $\dot{x}$, the space is often referred to as the phase-plane for the ADC. Once the coefficients, α_i, are determined for each basis function, it is possible to compensate the ADC by removing the error estimate from the data set as shown in (2).

$$z_i = x_i - e(x_i, y_i) \qquad (2)$$

*This work has been supported in part by the ARPA HBT/ADC program under a contract administered by the Office of Naval Research Grant N000149311007

In (2), z_i represents the compensated signal where x_i is the i^{th} sample of the ADC and y_i is the slope.

Previous publications have not addressed the issue of what type of basis functions should be used for this problem. Following neural network procedures for the development of training functions, two-dimensional Gaussian functions have been used in the past. These functions have consistently provided well-behaved solutions to the least square procedures used to estimate the ADC error function. The arbitrary use of these functions does not answer the question of whether there are specific functions that will more effectively model ADC error mechanisms. This paper presents some results that have been obtained in a preliminary look at choosing functions based upon different architectural features used in the design of ADCs.

Section II presents results obtained using specific basis functions to represent designated error features. In each case the effect of using a specific basis set is evaluated by using the error function thus obtained to compensate the ADC. The compensation performance is obtained by measuring the ADC's compensated spurious free dynamic range (SFDR) over the Nyquist band. It should be noted that each of the specific error functions are estimated by using the same calibration data set, thus not requiring any variations or special changes in the calibration circuitry. The results therefore show that a set of calibration data contains the information necessary to estimate particular error features whenever pertinent basis functions are used.

II. ADC Error Features

A. Hysteresis

A test used by ADC manufacturers is the measurement of differential nonlinearities. This test is performed by using a computer driven DAC to generate a precision ramp signal. The ramp takes a specified number of steps through each state of the ADC. The ADC is sampled several times at each step with the result that statistics can be assembled for each quantization interval and threshold [2, 3]. This test is virtually a static test except that the results differ for an upward versus a downward ramp. The measurement thus exhibits a hysteresis phenomenon for the

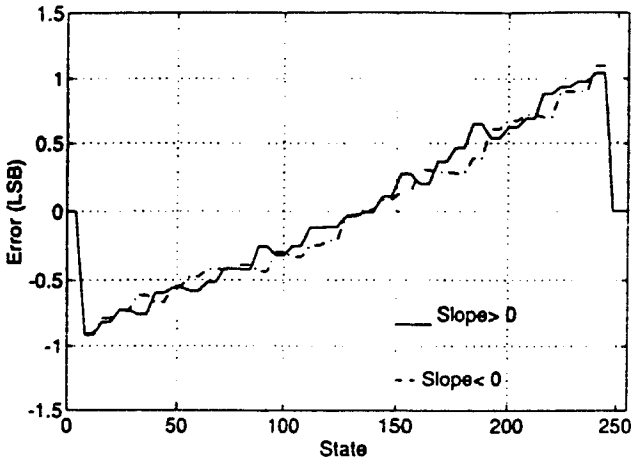

Figure 1: Flash converter dynamic hysteresis estimate

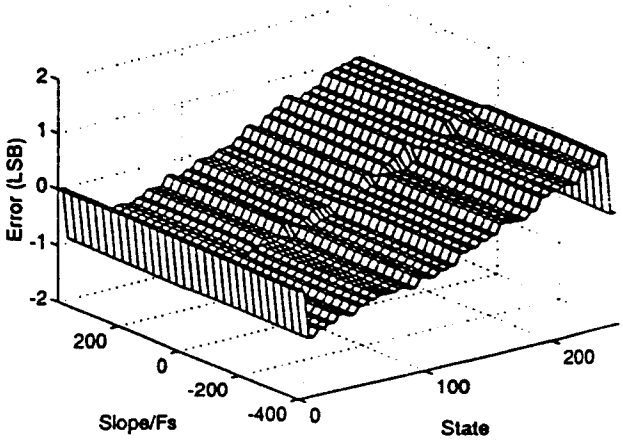

Figure 2: Hysteresis error function in $x - \dot{x}$ space

quantization threshold parameters.

It is possible to observe the same hysteresis by sampling a pure sine wave signal and constructing an error estimate using the dominant harmonic distortion terms found in the FFT of the sample set. When the error estimate is plotted versus the state of the ADC it is observed that the error forms an open contour thus illustrating hysteresis as a function of test frequency and ADC state. Hysteresis is a dynamic phenomenon and is measurable by using sinewave data as long as the selected basis functions allow for its representation. One way to allow the presence of hysteresis is shown in (3) using the unit step function.

$$\xi = u(y)f(x) + u(-y)g(x) \qquad (3)$$

The error in (3) is given by $f(x)$ when the ADC state is increasing and by $g(x)$ when it is decreasing. Thus (3) allows two distinct error functions based upon the slope of the ADC at any of its output states, x_i.

The hypothesis is tested by using 32 unit pulse functions for each of $f(x)$ and $g(x)$. The functions were uniformly centered over the 8-bit range of the TKAD20, each with a width of eight states. The resulting 64 coefficients, α_i, were estimated using least square methods [1] on the lowest frequency data of the calibration set; e.g., 2.5 MHz at two amplitudes and with error based upon the first 20 harmonics of each signal. The resulting dynamic hysteresis is shown in Fig.1. The solid curve is error (in LSBs) versus the ADC state for increasing state whereas the dashed curve is for decreasing states. A hysteresis phenomenon is definitely evident for this ADC. The corresponding error is shown as a two dimensional function in Fig.2. Clearly theres is no $\dot{x}$ dependence other than the "cut" at $\dot{x} = 0$ where the function switches from $g(x)$ to $f(x)$. The error table of Fig.2 is then used to compensate ADC samples.

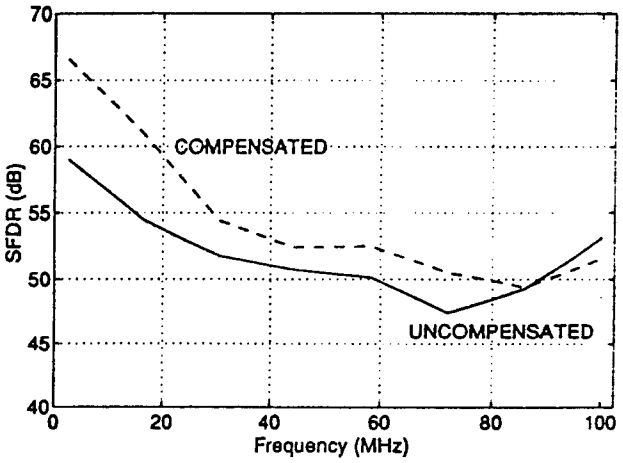

Figure 3: SFDR improvement using hysteresis errors

The performance improvement is illustrated by means of the measured SFDRs shown in Fig.3 where compensated and uncompensated SFDRs are compared. The graph shows that the hysteresis estimate improves low frequency performance by as much as 6 dB out to about 20% of the Nyquist band. This measure clearly shows the extent to which hysteresis is present and should be accounted for in order to improve the dynamic performance of this ADC.

B. Sample-time Error

Another important feature that contributes to ADC sample error is referred to as sample-time jitter. Almost all high-speed ADCs use some form of Sample/Hold (S/H) circuitry which can contribute to amplitude dependent sample-time errors. Various techniques are used to try and measure this phenomenon and most involve precision filters, phase-locking techniques, and special circuitry to

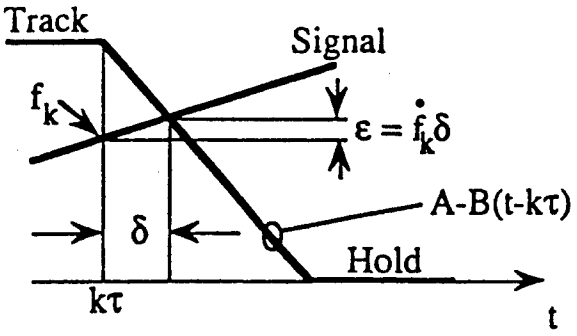

Figure 4: Sample-time error generated by S/H switching

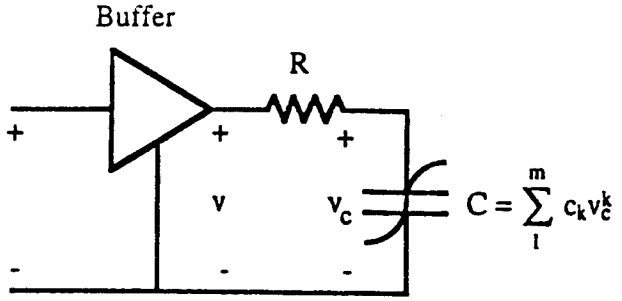

Figure 5: The buffer amplifier drives a nonlinear capacitor

isolate this second order effect. An analysis of the response diagram shown in Fig.4 leads to the following result.

As shown in Fig.4, the state of the ADC is compared to the S/H control signal used to control the switch. Most high-speed sample-holds employ current switching through diode bridge circuits and, as was originally shown by Gray and Kitsopoulas [4], the switch does not change state until some point after the command is initiated. The point is determined by the intersection of the desired signal with the switch transition.

Let x_k = ADC state at the sample time $k\tau$
y_k= corresponding slope
$A - B(t - k\tau)$= Switch transition waveform, then with
δ = sample-time error

we get (4) at the intersection of the two waveforms.

$$x_k + y_k\delta = A - B\delta \tag{4}$$

Rearrangement yields (5).

$$\delta = \frac{A - x_k}{B + y_k} \tag{5}$$

The error is given by δy_k so that (6) is obtained by invoking the fact that $B \gg yk$.

$$\xi = y_k \frac{A - x_k}{B} \tag{6}$$

(6) shows that sample-time errors yield a polynomial (albeit a straight line) in the ADC state variable times the corresponding slope. No higher order terms are involved for a high speed switch.

Before testing these error functions it is important to note that a similar result is obtained from any non-linear capacitance that is present in the signal path. Generally, flash comparators yield unavoidable non-linear capacitance at their input. When several (approaching 2^{Nbits}) of these are paralleled, it is difficult to avoid non-linear capacitance on the signal path. As shown in Fig.5, the static capacitance is modeled with a polynomial in the voltage variable, v_C across the capacitor. The voltage variable, v, at the buffer output, is the desired ADC state variable. Thus applying KCL at the capacitor yields (7).

$$\begin{aligned} G(v - v_C) &= G\xi = d(Cv_C)/dt \\ \xi &= R\left(\sum_{k=1}^{m}(k+1)C_k v_C^k\right)\dot{v_C} \end{aligned} \tag{7}$$

The result given in (7) is based on the assumption that ξ is small hence v_C is nearly equal to v and so we obtain the error form given in (8) for a nonlinear capacitor.

$$\xi = yp(x) \tag{8}$$

Nonlinear capacitance in the signal path yields an error basis function which includes the form just derived for amplitude dependent sample-time error.

A measured error function, using the full calibration data set is shown in Fig.6. A fifth order polynomial was used for $p(x)$ and no other basis functions were used to obtain the error table. Since the sample-time error is given by the slope times state, as used to derive (6), it is possible to use the error function to obtain an estimate of sample-time error as a function of ADC state. This result is shown in Fig.7. [thb]

In the mid-range of ADC values, which corresponds to small incremental signals, the sample-time error appears to have a linear slope thus indicating that the S/H error is dominant for small signals. As the signal is increased, the curve exhibits nonlinear behavior thus suggesting that the nonlinear capacitor dominates sample-time error for large signals. Note that errors ranging from zero to a few picoseconds are obtained from this result without having to resort to any special circuitry or test procedures.

Finally, the estimated sample-time error function is used to compensate the ADC to observe how this error representation affects performance. The result is shown

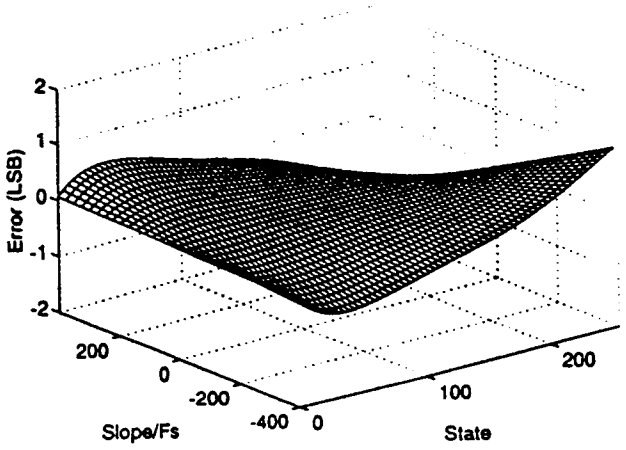

Figure 6: A slope dependent error table

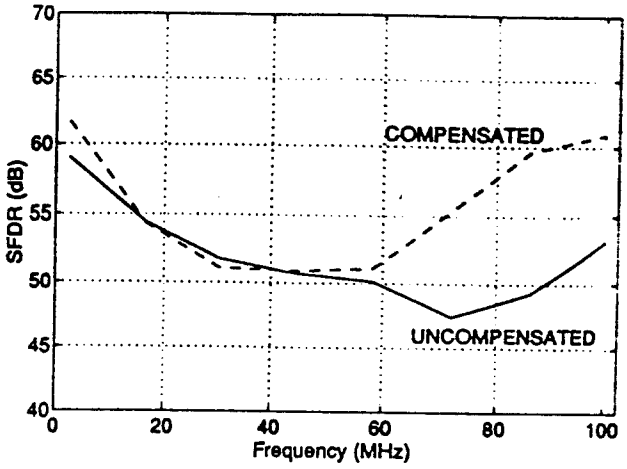

Figure 8: Improvement using sample-time errors

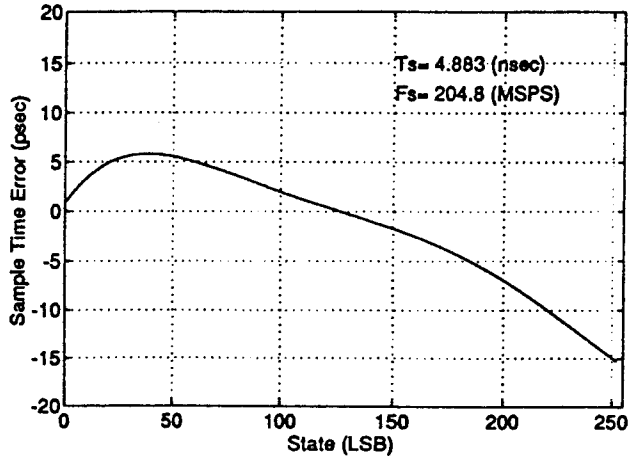

Figure 7: Estimated sample-time error

in Fig.8 where compensated and uncompensated SFDRs are compared. The graph shows that the sample-time error provides a significant contribution to dynamic performance for frequencies at the upper end of the Nyquist band. Sample-time error has negligible effect on low frequency performance of the ADC as expected since the parameter, y, goes to zero for low frequency signals.

III. Conclusions

This paper has introduced the concept that particular basis functions can be selected to measure specific ADC architectural error phenomena. An 8-bit wide-band flash converter was used to illustrate the estimation of both hysteresis and sample-time errors from a single set of calibration data merely by changing the basis functions used to build dynamic error functions. An analysis showed that non-linear capacitance yields an error function that includes the error function required for the estimation of sample-time errors due to S/H switching circuits. Hysteresis error modeling improved the ADC low frequency performance while sample-time and non-linear capacitor error modeling improved the high frequency performance.

Error phenomena considered in this paper did not contribute significantly to midband performance of the ADC. The use of two- dimensional Gaussian, or sinc, functions uniformly distributed over x, y space has historically provided significant improvement for the midband region of the ADC [1].

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Appendix 4

A copy of Paper No.4, *Measurement of Random Sample Time Jitter for ADCs*, by DM Hummels, et al, was submitted in Oct 1994 for presentation at the 1995 IEEE International Symposium on Circuits & Systems.

This paper presents initial results of methods developed to obtain statistical measures for ADC random error components.

Measurement of Random Sample Time Jitter for ADCs

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***Abstract*— This paper addresses the measurement of random sample-time jitter in the characterization of ADC's. A straightforward test is developed which allows for measurement of both additive noise power and RMS sample-time jitter. Simulations are used to assess the accuracy of the technique. Experimental results are also given for a commercially available ADC.**

I. Introduction

Analog-to-Digital Converters (ADC's) are often characterized in terms of the amount of noise which is introduced into the signal during the sampling process. Most ADC manufacturers provide specifications for the number of "effective bits" which the converter is providing. This specification includes the contribution due to a wide variety of noise sources, including thermal and shot noise in the input stages of the converter, errors in the quantization thresholds, and noise which is present on the clock signal.

For many applications, it is desirable to know not only the amount of noise which the converter is introducing, but also the source of the noise. From an ADC designer's point of view, knowledge of whether noise which is introduced through the input signal path, or through instability in the clock signal is critical to focusing the design effort. Similarly, users of ADC's need techniques to isolate noise sources. Converters may exhibit noise levels which are higher than the specifications predict either because of improperly driving the converter, or because of a loss of integrity in the sampling clock.

In this paper, a technique is presented which allows for the separation of additive noise sources from noise which is introduced through sample time jitter. The test is performed by driving the converter using a sinusoidal source, and removing all significant distortion that the converter introduces. The resulting noise process contains quantization noise, thermal noise from the converter input, and noise which is introduced from sample time jitter. In Section II we show that the sample-time jitter noise has a time-varying variance, since this noise signal is modulated by the derivative of the input signal. A procedure is introduced which measures the power in the modulated process, and relates this quantity to the RMS deviation in the sample time. Simulation results verifying the procedure are presented in Section III. Section IV presents measured results obtained using a commercially available 250 Msps converter.

It should be stressed that variations in the sampling instant which are related to the input signal may also result in distortion. In this paper we do not attempt to characterize the distortion which is introduce by misalignment of the clock signal. Rather, we are concerned with the measurement of the random component of the sample time deviations which contribute to the noise floor of the converter. Measurement of sample-time deviations which result in distortion introduced by the converter is discussed in another paper [1].

II. Formulation

Let $x(t)$ denote the input signal to an ADC. The output of the converter is a sequence of samples y_k, given by

$$y_k = x(kT_s + \Delta_k) + g(x(t))\,|_{t=kT_s} + n_k \qquad (1)$$

In (1), T_s represents the ideal sampling period for the converter, $g()$ represents a nonlinear function to model distortion which is introduced by the converter, and n_k denotes an additive noise component which is due to dithering, quantization noise, and noise sources in the input stage of the converter. The Δ_k term of (1) represents the (random) deviation in the sample time. Our goal is to identify techniques to estimate the variance of the random components Δ_k and n_k, denoted σ_Δ^2 and σ_n^2 respectively. The RMS sample-time jitter is the standard deviation of Δ_k, σ_Δ.

Note that in (1), the distortion function $g()$ may depend not only on $x(t)$ but also on the dynamic properties of $x(t)$ (its derivatives). The magnitude of $g()$ is generally kept

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small–on the order of an LSB. Also, manufacturers attempt to control the sampling instant so that Δ_k is small relative to the rate of change of the input signal. Using this fact, y_k may be accurately modeled in terms of the true sample value $x(kT_s)$ and an additive noise component.

$$y_k \approx x(kT_s) + \Delta_k \dot{x}(kT_s) + g(x(t))\,|_{t=kT_s} + n_k \qquad (2)$$

The key to separating the contribution to the noise floor due to Δ_k from that of n_k is to take advantage of the fact that Δ_k is modulated by the derivative of the input signal (errors introduced due to sample-time deviations are largest when the input signal is changing quickly). For measurement of the noise variance, we may drive the converter using a sinusoidal source.

$$\begin{aligned} x(t) &= A\cos(\omega_0 t + \theta) && (3)\\ y_k &= A\cos(\omega_0 kT_s + \theta) + g(x(t))\,|_{t=kT_s} \\ &\quad -A\omega_0\Delta_k \sin(\omega_0 kT_s + \theta) + n_k && (4)\end{aligned}$$

In this case, the distortion function $g()$ is periodic, so that the first line of (4) may be removed from the sample sequence $\{y_k\}$ by finding the FFT of the sequence, and excising all frequencies which are harmonics of the input frequency ω_0. Note that the Δ_k term of (4) is not removed by this process. This term is a random sequence with variance which is periodic at frequency ω_0. The resulting sequence (with periodic components removed) is

$$e_k = -A\omega_0\Delta_k \sin(\omega_0 kT_s + \theta) + n_k \qquad (5)$$

To estimate the variance of the components of (5), we square e_k and evaluate the expected value.

$$\begin{aligned} E\{e_k^2\} &= E\{A^2\omega_0^2\Delta_k^2 \sin^2(\omega_0 kT_s + \theta) + n_k^2\} \\ &= E\left\{\left(\frac{A^2\omega_0^2\Delta_k^2}{2} + n_k^2\right)\right. \\ &\quad \left. -\frac{A^2\omega_0^2\Delta_k^2}{2}\cos(2\omega_0 kT_s + 2\theta)\right\} && (6)\\ &= \left(\frac{A^2\omega_0^2\sigma_\Delta^2}{2} + \sigma_n^2\right) \\ &\quad -\frac{A^2\omega_0^2\sigma_\Delta^2}{2}\cos(2\omega_0 kT_s + 2\theta) && (7)\end{aligned}$$

The procedure for estimating the variance σ_Δ^2 is now apparent. The sequence $\{e_k^2\}$ contains a discrete frequency component at twice the test frequency which has magnitude proportional to the desired variance. Once σ_Δ^2 is known, the variance of the additive noise component σ_n^2 may be estimated from the DC component of $\{e_k^2\}$.

The procedure is summarized in the following steps:

1. Drive the converter input with a sinusoidal signal with frequency $\omega_0 = m(\omega_s/N)$, where $\omega_s = 2\pi/T_s$, N is the number of samples collected, and m is an integer. Selection of N as a power of 2, and m as an odd number makes the calculation of the FFT fast, and excites the converter uniformly across the desired states.

2. Collect N samples, $\{y_k : \quad k = 0, 1, \ldots, N-1\}$. Remove the periodic components of $\{y_k\}$ by taking an FFT, removing the DC, fundamental, and all significant harmonics of ω_0, and calculating the inverse tranform of the remainder. The resulting sequence is denoted $\{e_k\}$.

3. Evaluate the FFT of the sequence $\{e_k^2\}$.

$$E_n = \sum_{k=0}^{N-1} e_k^2 e^{-j2\pi nk/N} \qquad (8)$$

   Let C_0 denote the DC term of the signal ($C_0 = E_0/N$), and let C_2 denote the magnitude of the $2\omega_0$ term ($C_2 = 2|E_{2m}|/N$).

4. Calculate the desired estimates:

$$\begin{aligned} \hat{\sigma}_\Delta^2 &= \frac{2C_2}{A^2\omega_0^2} && (9)\\ \hat{\sigma}_n^2 &= C_0 - C_2 && (10)\end{aligned}$$

In step 4, the value of A may be obtained by observing the ω_0 term of the transform taken in step 2. While the theory holds for any input frequency, in practice ω_0 must be chosen large so that the $2\omega_0$ term of step 3 is well above the noise floor. Equation (7) predicts that the strength of the second harmonic term increases quadratically with ω_0.

III. Simulation Results

To test the accuracy of the estimation procedure, a simulation was developed which included a known amount of sample-time jitter. The equations giving the distortion terms of the ADC model are taken from [2]. Let x_1 denote the (dithered) sample $x(kT_s - \Delta_k) + d_k$, where d_k denotes a random dither component which is added to the signal prior to sampling in order to randomize the quantization error. The output of the converter is determined as follows:

$$\begin{aligned} x_2 &= a\tanh\left(\frac{x_1}{b}\right) && (11)\\ x_3 &= x_2 + c\dot{x}_2 - d|x_2|\dot{x}_2 && (12)\\ x_4 &= x_3 + \left[1 - \cosh\left(\frac{x_3}{e}\right)\right] && (13)\\ y_k &= Q(x_4) && (14)\end{aligned}$$

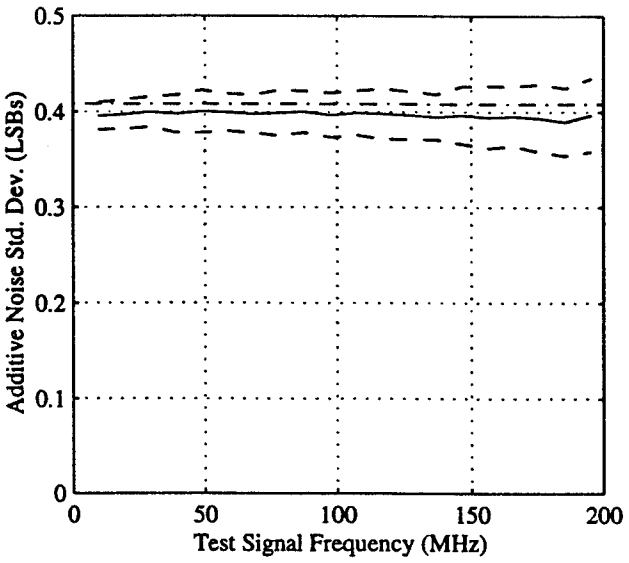

Figure 1: Estimation of σ_n. The solid line indicates the average estimate, and the dotted lines give ± 3 standard deviation bounds. The dash-dot line indicates the actual value of σ_n for the simulated ADC.

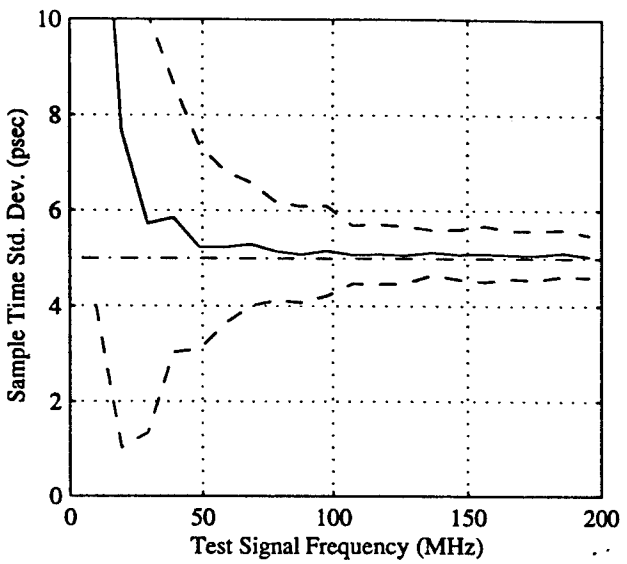

Figure 2: Estimation of σ_Δ. The solid line indicates the average estimate, and the dotted lines give ± 3 standard deviation bounds. The dash-dot line indicates the actual value of σ_Δ for the simulated ADC.

Equations (11) and (13) reflect amplitude distortion in the input and buffer amplifier stages of the converter. Deterministic sample-time offsets result in (12), which is derivable from a symmetrical quad-switching circuit following the analysis of Gray and Kistopoulas [3]. In (14), the function Q() is used to represent quantization to one of 2^n values for an n-bit converter.

All of the results presented here were for a simulated 8-bit converter sampling at 200 MSPS with a peak-to-peak full scale range of 2 V. The simulation parameters used were $a = b = 4$, $c = d = 3 \times 10^{-11}$, and $e = 7.25$. The parameters were chosen to give distortion terms which were roughly consistent with the measured distortion for the 8-bit converter tested in Section IV. The additive dither d_k was chosen to be a Gaussian random variable with variance equal to the quantization noise power. This gives a theoretical value of $\sigma_n = 1/\sqrt{6} = 0.4082$ LSBs. Δ_k was also chosen to be Gaussian, with standard deviation $\sigma_\Delta = 5$ psec. Test frequencies were varied from 10 MHz to 200 MHz with 50 trials at each frequency. For each trial, 4096 input samples were generated and used to form estimates of σ_n and σ_Δ. Step 2 of the estimation algorithm was implemented by removing the first 20 harmonics of the test signal frequency. Figures 1 and 2 illustrate the results. As expected, the estimate of σ_Δ improves with increasing test signal frequency, as the second harmonic term of (7) comes out of the noise floor. Both estimates appear to be nearly unbiased for large test signal frequencies.

IV. Experimental Results

The estimation procedure was implemented on a Tektronix AD-20 8-bit converter sampling at 204.8 MSPS. Examination of the spectrum (8) showed a significant component at $f_s/2$ in addition to the expected terms at DC and $2\omega_0$. The presence of this term suggested that the converter was actually a time-interleaved converter, employing two converters sampling alternately. To test the observation, the sample sequence was broken into two separate sequences–the first containing the odd numbered samples, and the second containing the even numbered samples. Each of these sample sequences displayed only the DC and $2\omega_0$ terms predicted in Section II.

The estimation algorithm was then implemented on each of these sub-sequences, resulting in two separate estimates of σ_n and σ_Δ. Step 2 of the algorithm was implemented by removing the largest 20 spurious signals in the transform of the sample sequence. Estimates were formed for input signal frequencies ranging from 100 MHz to 200 MHz (No significant $2\omega_0$ term was apparent at frequencies below 100 MHz). Input signal amplitudes were set at 95% of the full-scale range of the converter. In all cases the converter was dithered using Gaussian noise sources with 100 MHz bandwidth and noise power equal to the ideal quantization noise power. This gives a theoretical value for an ideal converter of $\sigma_n = 1/\sqrt{6} = 0.4082$ LSBs. Each estimate was obtained using 16384 samples (8192 samples per sub-sequence).

Figure 3 gives a plot of the second harmonic term C_2

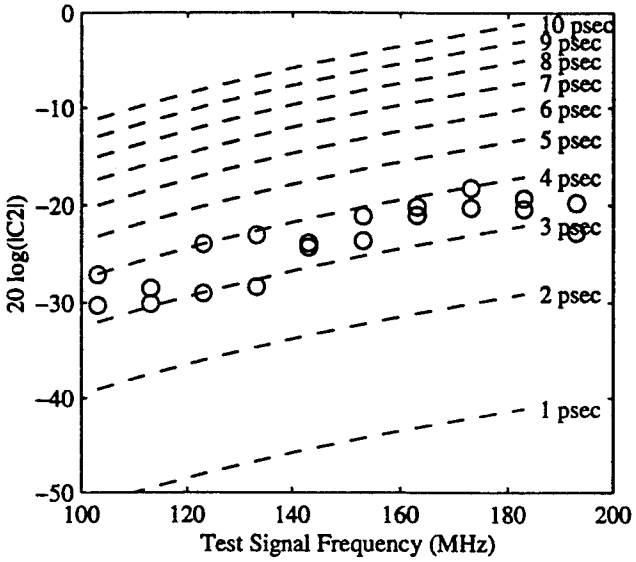

Figure 3: Measured magnitude of C_2 for various test frequencies. Dashed lines show the behavior predicted by the theoretical development for various values of σ_Δ.

from step 3 of the algorithm for the various test signal frequencies. Also shown are the theoretical curves for various values of σ_Δ which are prediced by equation (7). The plots show fairly consistent results, indicating that the quadratic behavior of C_2 as a function of ω_o is being observed.

The actual estimates of σ_n and σ_Δ are shown in Figures 4 and 5. Measured values of σ_n range consistently from 0.4 to 0.5 over the entire measurement band. These results are only slightly worse than those predicted for an ideal 8-bit converter, indicating a relatively low-noise converter. Sample time jitter measurements show sample time standard deviations on the order of 3 to 4 psec over the entire measurement band.

V. Conclusions

A straightforward test has been developed which allows for the measurement of random sample-time jitter in ADCs. The test is based on driving the converter using a high-frequency sinusoidal test signal. Simulation and experimental results have shown the test may provide accuracy on the order of 1 psec.

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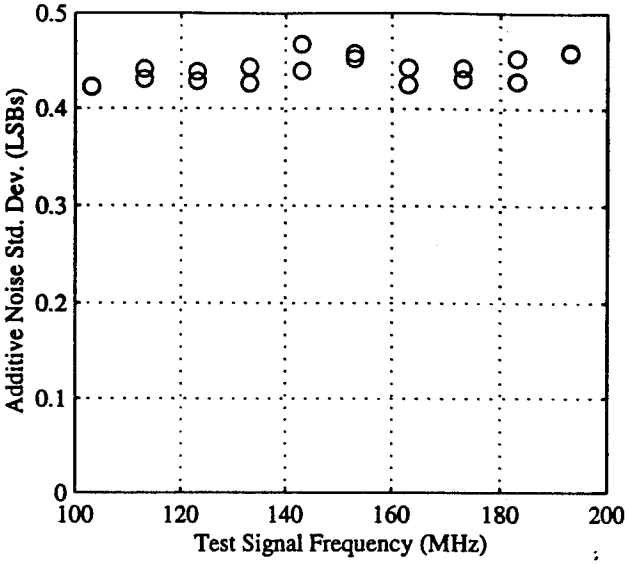

Figure 4: Measurement of σ_n for a Tek AD-20.

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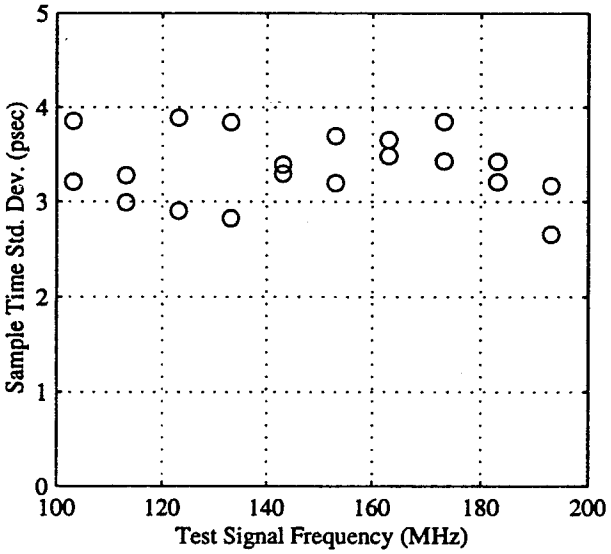

Figure 5: Measurement of σ_Δ for a Tek AD-20.